Analysis and Characterization of Four-quadrant Switches based Commutation Cell

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***Abstract*—A four-quadrant switch (FQS) blocks either polarity voltage and controls current flow in both directions. Unlike voltage-source converters, in which two-quadrant switches operate over a narrow voltage range, four-quadrant switches are required to operate over a wide range of both voltage and current in applications such as matrix converters and current-source converters. Furthermore, matrix converters require multi-step commutation schemes compared to two-step schemes for current-bidirectional switch based voltage-source converters and voltage-bidirectional switch based current-source converters. This paper provides a generalized overview of commutation schemes used for two and four quadrant switches based two-level commutation cells, identifies comparison indices for FQS commutation schemes, and discusses the need for adaptive commutation-step times for wide voltage and current variation applications. Also, the static and dynamic characteristics of 1.2 kV rated FQS implementations utilizing commercial SiC MOSFETs from four different manufacturers and novel monolithic SiC BiDirectional Field Effect Transistor (BiDFET) have been reported.**

***Index Terms*—Commutation cell, four quadrant switch, SiC Bidirectional FET, BiDFET, characterization, switching loss, dead time, overlap time, commutation scheme, matrix converter.**

I. Introduction

A four-quadrant switch (FQS) is the basic building block of two-level and three-level commutation cells used for realizing matrix [1], current-source, T-type, Vienna [2], auxiliary resonant commutated pole [3], hybrid third harmonic injection [4] and many other converter topologies. Conventionally, a combination of single-quadrant and two-quadrant switches is employed to realize the FQS, and back-to-back (B2B) connected SiC MOSFETs with anti-parallel JBS (Junction Barrier Schottky) diodes forms the lowest on-state voltage drop and switching loss discrete-devices-based solution for the applications requiring 1.2 kV breakdown voltage switch [5]. B2B MOSFETs can be connected in common-drain (CD) or common-source (CS) configurations. CD-FQS implementation has been shown to have higher turn-on losses and lower turn-off losses relative to CS-FQS [6]. A CD-FQS based three-phase converter design requires only five isolated gate driver power supplies compared to CS-FQS based implementation. Also, packaging B2B vertical MOSFET bare dies in CD is more reliable, as constituent FETs' drain terminals available on the bottom-side can be soldered together on a common copper pad rather than using unreliable wire bonds. Therefore, CD is the preferable FQS configuration, particularly for three-phase converters employing zero-voltage turn-on switching.

The SiC BiDFET device is the first monolithic SiC four-quadrant switch comprised of two constituent 1.2 kV 4H-SiC JBS-diode-embedded-power MOSFETs (JBSFETs) connected in a common-drain configuration [7]. At least four discrete devices will be required to achieve the same functionality as a single-chip BiDFET device. A monolithic FQS solution enables a lower device count, smaller commutation loop inductance, lesser wire bonds, simpler packaging steps, and consequently more reliable, power-dense modules and converters. The switching characteristics of about 50 mΩ on-resistance Gen-1 BiDFET (1.1 cm^2 total area with 0.45 cm^2 of active area for each internal JBSFET) was reported in [8]. Recently, a new version of BiDFET device has been developed to achieve about 25 mΩ on-resistance with same chip size. In Gen-2 BiDFET, the JBS diodes have been separated from MOSFET cells and placed at four corners of the chip.

This paper is organized as follows. A generalized overview of two-level commutation cells is provided in section II to highlight similarities and differences between two-quadrant and four-quadrant switches based commutation cells. A two-level commutation cell is simply called 'commutation cell' in this paper. Section III identifies the parameters useful for evaluating FQS commutation cell performance, and provides static and dynamic characterization data of six FQS implementations using switches shown in Table I. The commercial SiC FETs are the lowest on-resistance TO-247-4 package 1.2 kV rated switches available from respective manufacturers, which will

TABLE I: Switches selected for performance evaluation of 1.2 kV rated four-quadrant switches based commutation cell.

Manufacturer	Part Number
Wolfspeed	C3M0016120K
Infineon	IMZA120R007M1HXKSA1
Navitas	UF3SC120009K4S
Qorvo	G3R12MT12K
NCSU	Gen-1 BiDFET (two-dies in parallel)
NCSU	Gen-2 BiDFET

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be connected back-to-back in common-drain configuration for FQS implementation. Gen-1 and Gen-2 BiDFETs are single-chip FQSs fabricated at the six-inch commercial foundry, X-FAB, using the North Carolina State University (NCSU) PRECiSE^{TM} process [9]. A single-side cooled half-bridge module utilizing Epoxy-Resin Composite Dielectric (ERCD) based insulated metal substrate as reported in [10], has been used for packaging BiDFET dies.

II. Commutation Cell Analysis

A commutation cell consists of two switches, connecting a voltage-source, v to a current-source, i. It forms a fundamental block of power electronics converters. Depending on the converter operation, the switches must block positive, negative or either polarity voltage, and conduct positive, negative or either polarity current. Due to non-ideal implementation of semiconductor switches, different structure switches need to used. The required switch structure is determined by v-i quadrants that commutation cell need to operate in. This paper focuses on the switch structures based primarily on MOSFETs. Fig. 1 shows three types of commutation cells based on two-quadrant switches (current-bidirectional and voltage-bidirectional) and four-quadrant switches (bidirectional). The arrow in the MOSFET symbol represents its intrinsic body-diode, yet an anti-parallel diode is included in the symbol to represent the MOSFET body diode. This is done to clearly highlight the duration for which body-diode conducts current or blocks voltage. This diode can also represent the anti-parallel JBS diode used for reducing hard turn-on switching loss in some applications.

Commutation refers to the process of transferring current-source from one voltage-source terminal to another. The mid-point voltage will have a positive or negative voltage edge depending on the voltage-source terminals' polarities. During commutation, two constraints must be met at all the times. Firstly, there must be a path for the current-source. Secondly, the voltage-source must not be short-circuited. Because of these constraints and different structures of two-quadrant and four-quadrant switches, the required commutation scheme (MOSFETs' gate-signals switching sequence) will be different for each commutation cell type. Also, the gate signal of a MOSFET only controls the current flow through its channel, while its intrinsic body-diode may conduct current contingent on the cell operating condition. When body-diode is conducting prior to gate signal switching, there is no voltage-current

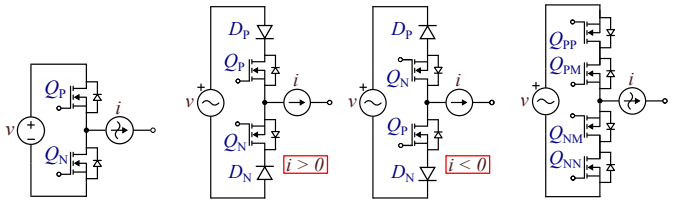


Fig. 1: Types of commutation cells: (a) current-bidirectional, (b) voltage-bidirectional, and (c) bidirectional.

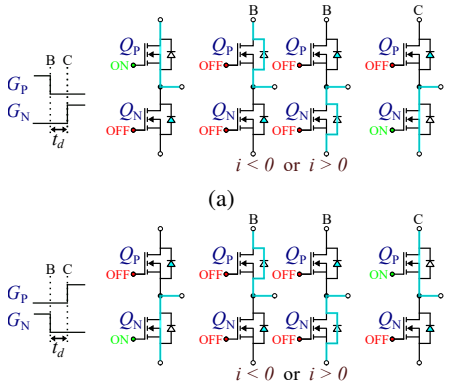


Fig. 2: Current-bidirectional commutation cell commutation process for: (a) -ve mid-point voltage-edge, (b) +ve mid-point voltage-edge.

crossover loss (soft-switching) in the switch as its voltage is clamped to body-diode on-state voltage drop during switching. This soft-switching is experienced by incoming switch when the cell mid-point voltage-edge and current source polarities are opposite, and outgoing switch otherwise. This condition is independent of commutation cell type, but the commutation scheme step at which current transfers from one voltage-source terminal to another can be different for each commutation cell type. To understand the similarities and differences in the operation of three commutation cell types, a generalized overview of the commutation schemes along with a study of switching transitions in each case is discussed below.

A. Current-bidirectional commutation cell

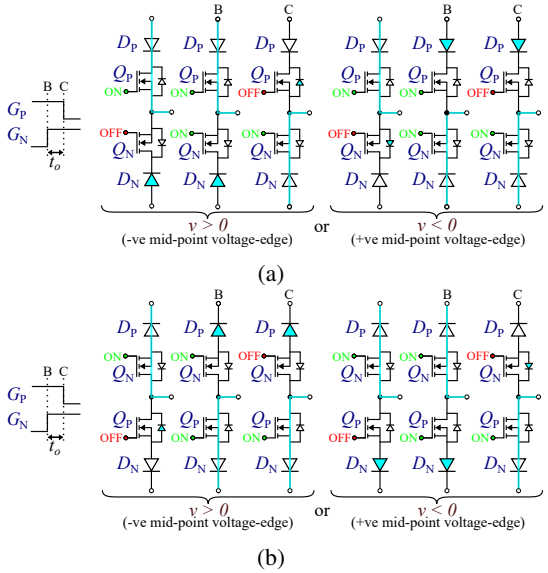
A current-bidirectional switch can block positive voltage and conduct either polarity current. It is used for DC/DC and voltage-source AC/DC converters. The commutation scheme for current-bidirectional commutation cell is shown in Fig. 2. The blue line denotes the current flow path and the diode highlighted in blue is the one blocking the voltage, v. The scheme involves turning off the outgoing switch gate (step B), followed by a dead-time, t_d to provide time for outgoing switch turn-off process and incoming switch output capacitance discharge in soft turn-on conditions, and finally turning on the incoming switch gate (step C). This scheme is independent of current polarity as switches' body-diodes provide a path for current flow at all the times. The current transfer between voltage-source terminals happens at step B or C depending on the mid-point voltage-edge and current-source polarities (step B when polarities are different and step C when polarities are same). Current transfer at step B causes hard turn-off of outgoing switch but facilitates ZVS (Zero Voltage Switching) turn-on of incoming switch. While, without current transfer at step B, outgoing switch undergoes ZVS turn-off, but incoming switch experiences hard turn-on at step C. The reverse-recovery current of outgoing switch body-diode increases the incoming switch's hard turn-on switching loss. This loss can be reduced by using anti-parallel JBS diodes or replacing MOSFETs with JBSFETs consisting of

monolithically integrated SiC MOSFET and JBS diode [11]. JBSFET occupies a lower semiconductor area, suppresses current flow through P-i-N body diode, and provides superior short-circuit performance compared to a MOSFET with anti-parallel JBS diode [12].

B. Voltage-bidirectional commutation cell

A voltage-bidirectional switch can block either polarity voltage and conduct single polarity current. It is used for current-source AC/DC converters, and can be implemented using a MOSFET with anti-series diode or MRBT (Monolithic Reverse Blocking Trasistor). An MRBT is a recently developed 1.2 kV rated voltage-bidirectional switch created by monolithic integration of SiC MOSFET and anti-series JBS diode [13]. Different voltage-bidirectional commutation cells are required for each current polarity as shown in Fig. 1b.

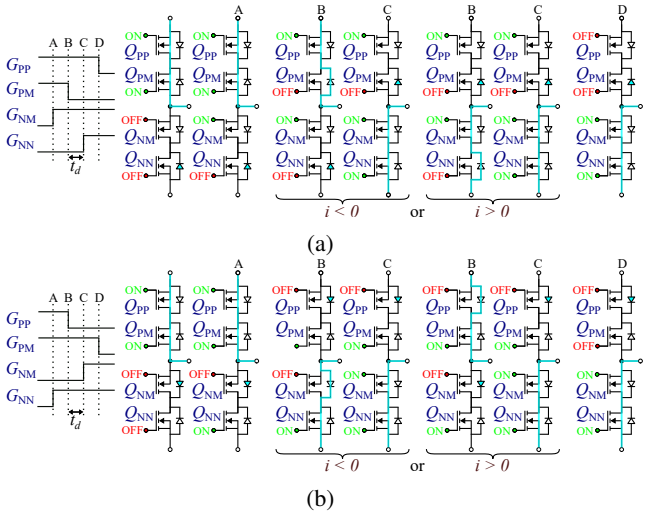
The commutation scheme as shown in Fig. 3 involves turning on the incoming switch gate (step B), followed by a overlap-time, t_o to provide time for incoming switch turn-on process and outgoing switch output capacitance discharge in soft turn-off conditions, and finally turning off the outgoing switch gate (step C). This scheme is independent of voltage polarity as anti-series diodes block either voltage polarity at all the times. The current transfer happens at step C when mid-point voltage edge and current-source polarities are opposite and at step B otherwise. With current transfer at step B, incoming switch suffers hard turn-on but facilitates ZCVS (Zero Current-Voltage Switching) turn-off of outgoing switch. Without current transfer at step B, incoming switch has ZCVS turn-on but outgoing switch undergoes hard-off at step C. Therefore, voltage-bidirectional commutation cell has similar switching losses as current-bidirectional commutation cell, but current transfer happens at different step for same operating conditions. ZVS involves current flow transfer between MOSFET channel and its body-diode at a rate dependent on gate current and MOSFET transconductance, while ZCVS occurs



(a)

(b)

Fig. 3: Voltage-bidirectional commutation cell commutation process for: (a) i $>$ 0, and (b) i $<$ 0.



(a)

(b)

Fig. 4: Voltage polarity based bidirectional commutation cell commutation process for: (a) v $>$ 0 (-ve mid-point voltage-edge), and (b) v $<$ 0 (+ve mid-point voltage-edge).

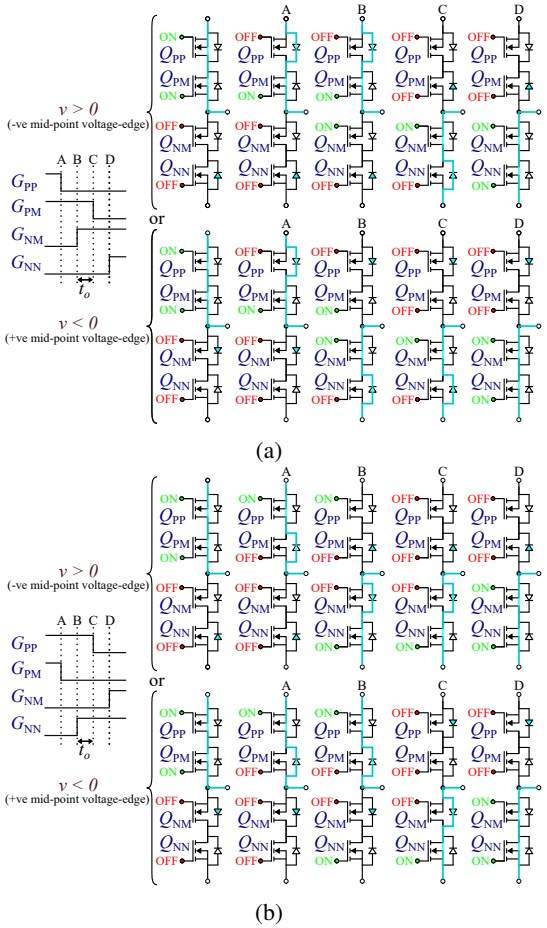
at zero current. Both ZVS and ZCVS will have no voltage-current crossover loss, but only ZVS will have MOSFET conduction loss dependent on on-state resistance, body-diode on-state voltage-drop and rate of transfer of current between MOSFET's channel and body-diode.

The reverse-recovery current of series diode increases the MOSFET switching loss during hard turn-on transitions. Therefore, series diode needs to be a low or zero reverse recovery charge diode like JBS diode. Also, at hard turn-off transition, the series diode of outgoing switch stops conducting current as MOSFET is turned off at step C, but the diode is still forward-biased. This diode will undergo reverse recovery or output capacitor charging whenever v polarity reverses. For a P-i-N series diode, the change in amount of its stored charge with the duration for which it is kept forward-biased without any current flow needs to be investigated. The MOSFET body-diode does not conduct current in any operating condition, hence, its reverse-recovery behavior has no affect on the converter performance.

C. Bidirectional commutation cell

A four-quadrant (or bidirectional) switch can block either polarity voltage and current. It is used for matrix converters and current-source AC/DC converters, and can be implemented using anti-series MOSFETs or BiDFET (BiDirectional Field Effect Transistor) consisting of monolithically integrated anti-series JBSFETs in common-drain configuration [7], [5]. To meet the commutation cell constraints, the constituent FETs of bidirectional switch cannot be switched together for commutation process. Consequently, multi-step commutation schemes involving independent control of constituent FETs' gate signals have been devised in the literature [14], [15].

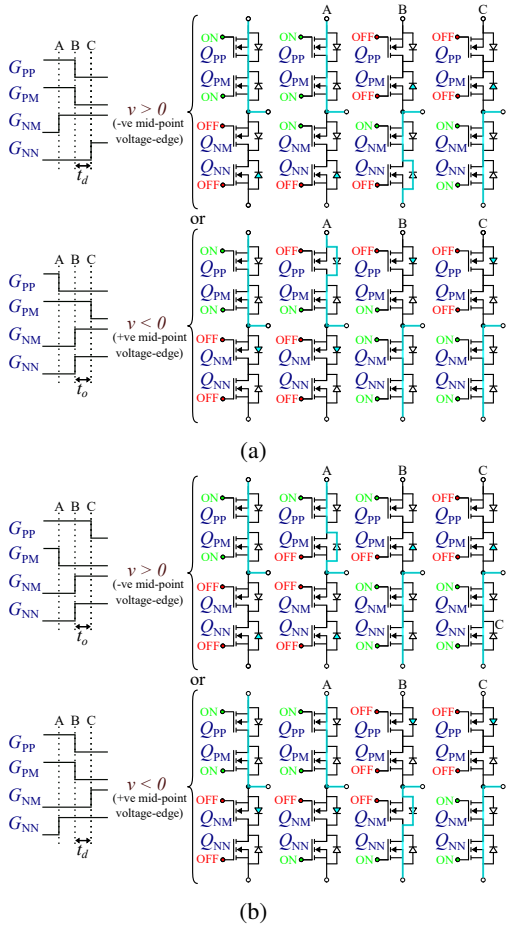
1) Voltage polarity based commutation scheme: With known v polarity, a current-independent four-step commutation scheme similar to that used for current-bidirectional commutation cell can be implemented, as shown in Fig. 4. The



(a)

(b)

Fig. 5: Current polarity based bidirectional commutation cell commutation process for: (a) i $>$ 0, and (b) i $<$ 0.



(a)

(b)

Fig. 6: Voltage and current polarities based bidirectional commutation cell commutation process for: (a) i $>$ 0, and (b) i $<$ 0.

current transfer happens at steps B or C only and switching losses of involved switches are similar to switches in current-bidirectional commutation cell. Switches involved in steps A and D undergo ZCVS. The body-diode of one of the constituent FETs conducts from step B to end of turn-off process at step C.

2) Current polarity based commutation scheme: With known i polarity, a voltage-independent four-step commutation scheme similar to that used for voltage-bidirectional commutation cell can be implemented as shown in Fig. 5. The current transfer happens at steps B or C only and switching losses of involved switches are similar to switches in voltage-bidirectional commutation cell. Switches involved in steps A and D undergo ZVS. The body-diode of one of the constituent FETs conducts during the whole commutation process from step A to end of turn-on process at step D.

3) Voltage and current polarities based commutation scheme: When both i and v polarities are known, a three-step commutation scheme can be implemented as shown in Fig. 7. This commutation scheme is dependent on both v and i polarities, but assures current transfer at step B for all operating conditions and has lower total commutation process time. The current transfer involves simultaneous switching of constituent FETs of outgoing or incoming switch depending on mid-point voltage-edge and current-source polarities (incoming switch when polarities are same and outgoing switch when polarities are opposite).

4) Comparison of commutation schemes: The three commutation schemes for bidirectional commutation cell based on sensed polarities of either or both voltage and current will cause same amount of total voltage-current crossover switching loss during commutation process, for the same operating conditions. The commutation cell undergoes soft turn-on and hard turn-off switching when mid-point voltage-edge and current-source polarities are different, and undergoes hard turn-on and soft turn-off switching when mentioned polarities are same. Soft turn-on and hard turn-off switching will have lower losses for MOSFET based commutation cells as hard turn-off switching loss is usually smaller than hard turn-on switching loss for MOSFETs. While commutation cells based on B2B IGBTs with anti-parallel diodes might have higher hard turn-off switching loss than hard turn-on switching loss, hence, operating conditions facilitating hard turn-on and soft turn-off switching should be preferred in this case.

The parameters different for commutation schemes include total duration required for completing commutation process, duration for which one of the constituent FETs' body-diode

TABLE II: Generalized overview of commutation schemes for different commutation cells.

Commutation cell		Mid-point voltage-edge polarity	Current source polarity	Current transfer step	Turn-on transition	Turn-off transition	Total commutation process duration	MOSFET body-diode conduction duration
Current-bidirectional		+	+	C	Hard	ZVS	t_{BC} ($\geq t_{ZVS\text{-}off}$) + $t_{hard\text{-}on}$	Total commutation process duration
		+	-	B	ZVS	Hard	t_{BC} ($\geq t_{hard\_off}$) + $t_{ZVS\text{-}on}$	
		-	+	B	ZVS	Hard	t_{BC} ($\geq t_{hard\_off}$) + $t_{ZVS\text{-}on}$	
		-	-	C	Hard	ZVS	t_{BC} ($\geq t_{ZVS\text{-}off}$) + $t_{hard\text{-}on}$	
Voltage-bidirectional		+	+	B	Hard	ZCVS	t_{BC} ($\geq t_{hard\text{-}on}$) + t_{ZCVS_off}	Zero
		+	-	C	ZCVS	Hard	t_{BC} ($\geq t_{ZCVS\text{-}on}$) + t_{hard_off}	
		-	+	C	ZCVS	Hard	t_{BC} ($\geq t_{ZCVS\text{-}on}$) + t_{hard_off}	
		-	-	B	Hard	ZCVS	t_{BC} ($\geq t_{hard\text{-}on}$) + t_{ZCVS_off}	
Bidirectional	**Known voltage polarity**	+	+	C	ZCVS at A and hard at C	ZVS at B and ZCVS at D	t_{AB} ($\geq t_{ZCVS\text{-}on}$) + t_{BC} ($\geq t_{ZVS\_off}$) + t_{CD} ($\geq t_{hard\text{-}on}$) + $t_{ZCVS\text{-}off}$	t_{BC} ($\geq t_{ZVS\text{-}off}$) + $t_{hard\text{-}on}$
		+	-	B	ZCVS at A and ZVS at C	Hard at B and ZCVS at D	t_{AB} ($\geq t_{ZCVS\text{-}on}$) + t_{BC} ($\geq t_{hard\_off}$) + t_{CD} ($\geq t_{ZVS\text{-}on}$) + $t_{ZCVS\text{-}off}$	t_{BC} ($\geq t_{hard\_off}$) + $t_{ZVS\text{-}on}$
		-	+	B	ZCVS at A and ZVS at C	Hard at B and ZCVS at D	t_{AB} ($\geq t_{ZCVS\text{-}on}$) + t_{BC} ($\geq t_{hard\_off}$) + t_{CD} ($\geq t_{ZVS\text{-}on}$) + $t_{ZCVS\text{-}off}$	t_{BC} ($\geq t_{hard\_off}$) + $t_{ZVS\text{-}on}$
		-	-	C	ZCVS at A and hard at C	ZVS at B and ZCVS at D	t_{AB} ($\geq t_{ZCVS\text{-}on}$) + t_{BC} ($\geq t_{ZVS\_off}$) + t_{CD} ($\geq t_{hard\text{-}on}$) + $t_{ZCVS\text{-}off}$	t_{BC} ($\geq t_{ZVS\text{-}off}$) + $t_{hard\text{-}on}$
	Known current polarity	+	+	B	Hard at B and ZVS at D	ZVS at A and ZCVS at C	t_{AB} ($\geq t_{ZVS\text{-}off}$) + t_{BC} ($\geq t_{hard\_on}$) + t_{CD} ($\geq t_{ZCVS\text{-}off}$) + $t_{ZVS\text{-}on}$	Total commutation process duration
		+	-	C	ZCVS at B and ZVS at D	ZVS at A and Hard at C	t_{AB} ($\geq t_{ZVS\text{-}off}$) + t_{BC} ($\geq t_{ZCVS\text{-}on}$) + t_{CD} ($\geq t_{hard\text{-}off}$) + $t_{ZVS\text{-}on}$	
		-	+	C	ZCVS at B and ZVS at D	ZVS at A and Hard at C	t_{AB} ($\geq t_{ZVS\text{-}off}$) + t_{BC} ($\geq t_{ZCVS\text{-}on}$) + t_{CD} ($\geq t_{hard\text{-}off}$) + $t_{ZVS\text{-}on}$	
		-	-	B	Hard at B and ZVS at D	ZVS at A and ZCVS at C	t_{AB} ($\geq t_{ZVS\text{-}off}$) + t_{BC} ($\geq t_{hard\_on}$) + t_{CD} ($\geq t_{ZCVS\text{-}off}$) + $t_{ZVS\text{-}on}$	
	Known voltage and current polarities	+	+	B	One ZVS and other hard at B	ZVS at A and ZCVS at D	t_{AB} ($\geq t_{ZVS\text{-}off}$) + t_{BC} ($\geq t_{hard\text{-}on}$) + $t_{ZCVS\text{-}off}$	t_{AB} ($\geq t_{ZVS\text{-}off}$) + $t_{hard\text{-}on}$
		+	-	B	ZCVS at A and ZVS at C	One ZVS and other hard at B	t_{AB} ($\geq t_{ZCVS\text{-}on}$) + t_{BC} ($\geq t_{hard\text{-}off}$) + $t_{ZVS\text{-}on}$	t_{BC} ($\geq t_{hard\text{-}off}$) + $t_{ZVS\text{-}on}$
		-	+	B	ZCVS at A and ZVS at C	One ZVS and other hard at B	t_{AB} ($\geq t_{ZCVS\text{-}on}$) + t_{BC} ($\geq t_{hard\text{-}off}$) + $t_{ZVS\text{-}on}$	t_{BC} ($\geq t_{hard\text{-}off}$) + $t_{ZVS\text{-}on}$
		-	-	B	One ZVS and other hard at B	ZVS at A and ZCVS at D	t_{AB} ($\geq t_{ZVS\text{-}off}$) + t_{BC} ($\geq t_{hard\text{-}on}$) + $t_{ZCVS\text{-}off}$	t_{AB} ($\geq t_{ZVS\text{-}off}$) + $t_{hard\text{-}on}$

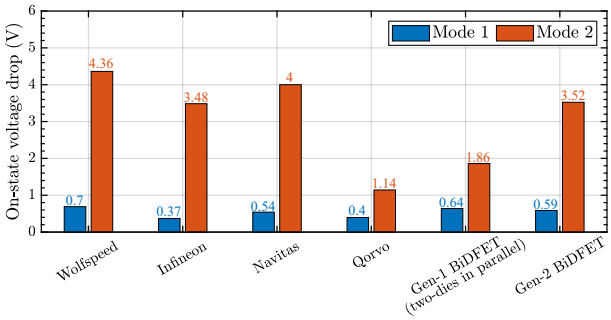
conducts current, and predictability of current transfer step as shown in Table II. The total commutation process duration limits the maximum frequency of the commutation cell, body-diode voltage-drop increases switch conduction losses, and current transfer at predictable commutation step allows simpler compensation of switches' duty ratios originally calculated for ideal switching case. This compensation is needed for precise control of commutation cell mid-point volt-seconds and charge going into each voltage-source terminal. For converter topologies having matrix converter connected across a high-frequency transformer, like single-stage single-phase AC/DC converter [16], unequal volt-seconds during positive and negative switching cycle may cause high-frequency transformer core saturation. Also, unequal charge into voltage-source terminals during positive and negative grid-frequency cycles will cause DC current injection into the grid, which might lead to saturation of the magnetic core of local line-frequency transformer connected to the grid.

III. Characterization of Bidirectional Commutation Cell

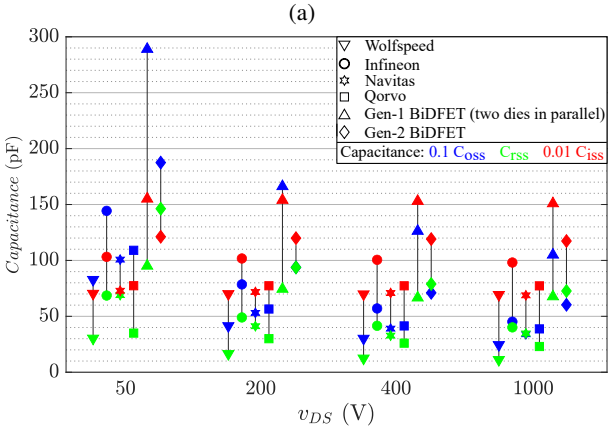
Based on the type of commutation scheme, commutation cell mid-point voltage-edge polarity and current-source polarity, an FQS switch may have either or both constituent FETs conducting or switching at any instant in time. To facilitate the performance analysis of bidirectional commutation cell based converters, FQS steady-state and switching characteristics need to be evaluated for all modes of operation. Matrix converters connected to ac grid or motor drives require switches to operate over a wide range of both voltage and current during each grid or motor frequency cycle. This is unlike voltage-source converters, in which switches operate over a narrow DC bus voltage range. Thus, the MOSFET characteristics usually assessed at a fixed voltage must be examined across a wide voltage range.

A. On-state voltage drop

The FQS may conduct current with both constituent FETs gates turned on (Mode 1), or just one constituent FET gate turned on (Mode 2). On-state voltage drop values for different FQS implementations at 20 A, as shown in Fig. 7a, have been measured using Keysight B1505A Curve Tracer. Both constituent FETs' gate voltages are kept 15 V for Mode 1 testing, while one constituent FET's gate voltage is reduced to -3 V for Mode 2 testing. BiDFETs have been designed for 20 V/ -5 V nominal gate voltage rating, but have been tested at lower gate voltages to show performance at the same gate voltages as commercial MOSFETs. BiDFET's Mode-1 on-state voltage drop will reduce further with increase in gate voltage. SiC MOSFETs from Wolfspeed, Infineon and Navitas consist of SiC P-i-N body diodes. SiC FET from Qorvo is a



(a)



(b)

Fig. 7: (a) FQS on-state voltage drop at 20 A, and (b) FQS constituent FET capacitances variation with v_{DS}.

cascode circuit configuration having normally-on SiC JFET co-packaged with a low-voltage Si MOSFET. Hence, Si P-i-N diode conducts during third-quadrant operation of Qorvo SiC FET, whose voltage-drop is lower than SiC diode primarily due to lower voltage rating. Gen-1 BiDFET constituent JBSFETs intrinsic anti-parallel JBS diodes have lower knee voltage than SiC P-i-N diodes of same voltage rating [11]. Two versions of Gen-2 BiDFET were developed, one with anti-parallel P-i-N diodes and other with anti-parallel JBS diodes. This paper presents characteristics of Gen-2 BiDFET with anti-parallel P-i-N diodes.

B. Capacitances

This paper considers only common-drain configuration based FQS implementations. Hence, only constituent FETs' capacitances variation with drain-source voltage need to be considered, as shown in Fig. 7b. The capacitances were measured using Keysight B1505A Curve Tracer. The C_{rss} values for Qorvo SiC FET have been taken from its datasheet.

C. Switching transition times

Table II shows six types of switching transitions. The variation of each transition time with current and voltage need to evaluated. For same gate resistances and operating condition, gate charging-discharging times till threshold gate voltage remain constant, but the current transfer and drain-source voltage charge-discharge times depend on the type of switching transition.

ZCVS transitions only involve gate charging, hence there is no variation with voltage or current. The ZCVS transition time depends on FET input capacitance, and gate turn-on and turn-off resistances. During ZVS transition, the switch voltage is clamped to body-diode voltage drop. So, there is no variation in t_{ZVS} with voltage but time required for current transfer between body-diode and channel vary with current. Current transfer time should change almost linearly with current as di/dt depends only on MOSFET transconductance and rate of change of gate voltage, which in turn is controlled by turn-on and turn-off gate resistances. Hard-turn off transition time has two parts, first for charging the outgoing switch voltage and second for current transfer. During hard turn-off outgoing switch output capacitance, C_{oss} charges through current-source, therefore voltage-charging time is dependent on current-source magnitude. The C_{oss} value increases with decreasing voltage, so dv/dt slope increases as voltage rises during the charging process at constant current. Current transfer time is dependent on turn-off di/dt, which is controlled by MOS transconductance and turn-off gate resistance. As switch capacitance increases with decreasing voltage, current-transfer time should increase with decreasing voltage for same current. The turn-off di/dt causes overvoltage across the outgoing switch due to voltage drop across commutation loop parasitic inductance. Hard turn-on transition time also has two parts, first for current transfer and second for discharging the incoming switch C_{oss}. Both current transfer and voltage discharge are controlled by MOSFET transconductance and gate resistance. FET incurs additional losses as C_{oss} discharges through the FET channel. The current transfer time increases with increasing current and decreasing voltage, while voltage discharge time increase with increasing voltage and is independent of current. The overvoltage across the outgoing switch is caused by the rate of fall of body-diode reverse-recovery current from peak negative value to zero.

D. Body-diode turn-off behavior

Independent of commutation scheme, outgoing FET's body-diode conducts for $t_{ZVS-off}$ before incoming FET's hard turn-on switching. The selection of this time interval is critical, as body-diode reverse recovery charge increases with increasing body-diode conduction time, which causes higher current spikes and reverse-recovery time [17]. Hard turn-off takes longer time than ZVS turn-off, so if dead-time is set to be constant according to the hard turn-off condition, hard turn-on switching loss will be worse. JBS diode capacitive charge has been reported to be independent of its conduction time [18]. Further, as discussed in section II-B for voltage-bidirectional commutation cell, with current polarity based commutation scheme for bidirectional commutation cell, the current through body-diode becomes zero when series MOSFET is turned-off and no path is available for body-diode reverse recovery current. The body-diode undergoes reverse-recovery when voltage polarity changes. The JBS diode only has capacitive charge, but for P-i-N body diode, the variation of stored charge with the time for which it is kept forward-biased after current

through it becomes zero without incurring reverse-recovery needs to be investigated.

E. Switching energy loss

FQS constituent FETs undergo ZVS, ZCVS or hard switching. As only hard switching incurs losses, only hard turn-on (E_{on}) and hard turn-off (E_{off}) energy losses need to evaluated. This can be done by using the same double pulse test procedure used for two-quadrant switches as shown in Fig. 8a. Compared to two-quadrant switches commutation cells, bidirectional commutation cell has significantly higher parasitic inductance if FQS is implemented with discrete MOSFETs, but similar parasitic inductance if FQS is implemented with BiDFET. The higher parasitic inductance decreases the turn-on switching energy as the parasitic inductor voltage drop, Ldi/dt subtracts from voltage-source voltage during current rise time and reduces the incoming switch v_{DS} for miller plateau region, and hence decreases voltage-current crossover loss. But turn-off switching energy increases as voltage across outgoing switch rises to $v+Ldi/dt$ at the end of miller plateau region, which increases voltage-current crossover loss during current transfer time. The percentage change in switching energy caused by parasitic inductance might be similar at turn-on and turn-off, but absolute change is much higher for turn-on energy as it's value is usually much higher than turn-off energy and has higher variation with voltage. Therefore, absolute values of switching energies can only be compared for FQS implementations using same PCB layout (comparison of commercial FETs with each other and BiDFET modules with each other, not commercial FETs with BiDFET), but the rate of change of switching energies with current and voltage values can be compared for all FQS implementations. Fig. 8b-8c show the PCBs built for dynamic characterization of different FQS implementations, one for back-to-back connected commercial SiC MOSFETs and other for Gen-1 and Gen-2 BiDFET modules. Both PCBs have same decoupling capacitors, inductance and gate voltages (+15 V/-3 V), but parasitic inductance for B2B FQS based PCB is higher due to TO-247 package lead inductances. The FETs gate resistances are chosen to have almost same value di/dt transitions for all switches at 400 V, 20 A. Due to higher parasitic inductance, overvoltages across the outgoing switch are higher in B2B FQS commutation cell as shown in Fig. 9.

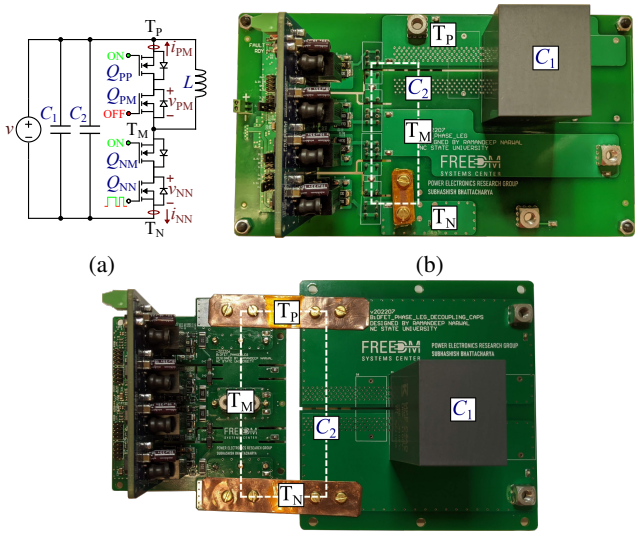


Fig. 8: (a) Double pulse test setup (L = 93.5 μH, C_1 = 25 μF, C_2 = 4 x 100 nF), (b) Back-to-back TO-247-4 package SiC MOSFETs based half-bridge PCB, and (c) BiDFET half-bridge module PCB. Dotted lines indicate commutation loop.

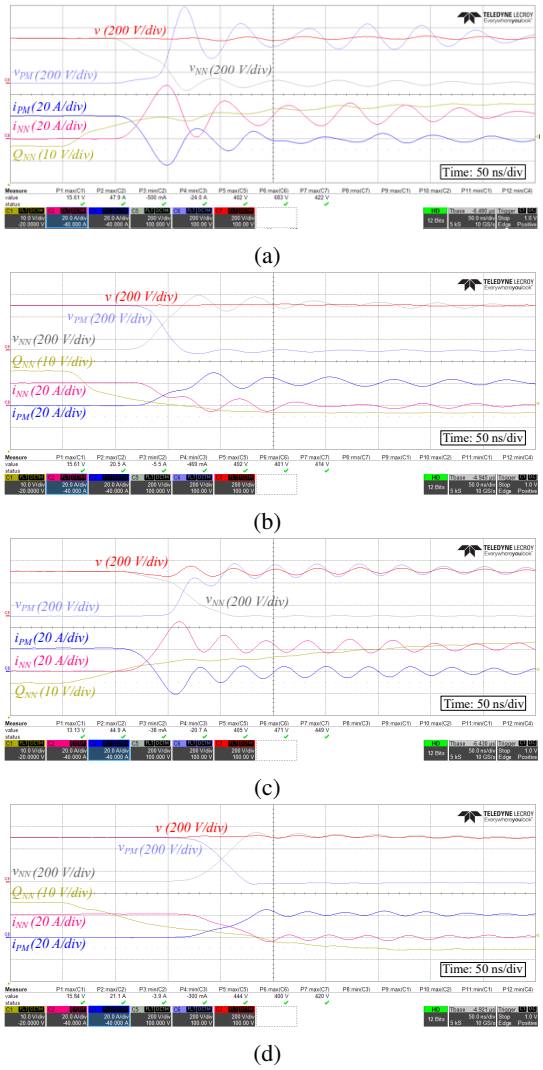
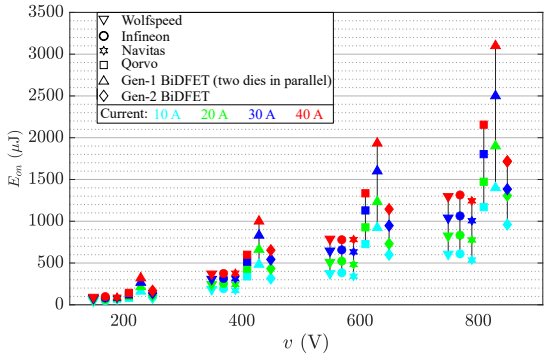
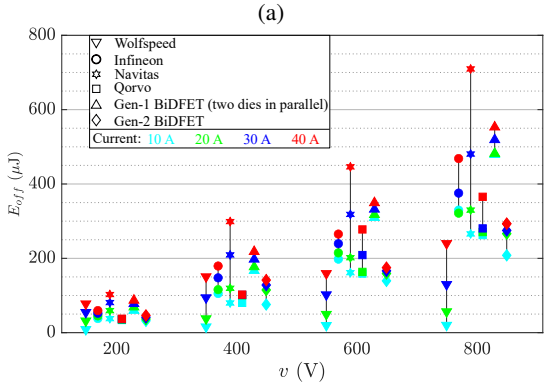


Fig. 9: (a) Switching waveforms at 400 V, 20 A for: (a) B2B Infineon turn-on, (b) B2B Infineon turn-off, and (c) Gen-2 BiDFET turn-on, and (d) Gen-2 BiDFET turn-off.

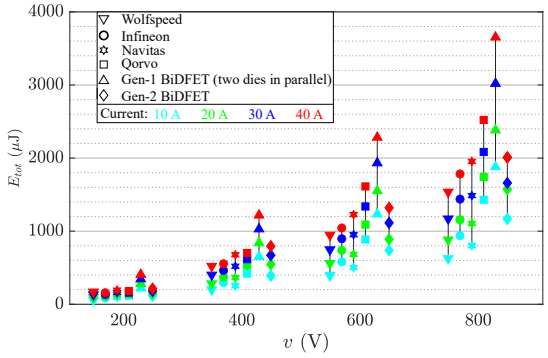
The variation of hard turn-on losses with current is expected to be higher for SiC MOSFETs based FQSs, as their body-diode stored charge varies with current, turn-on di/dt and dead-time, while capacitive energy required for JBS diodes in BiDFETs doesn't change with current or turn-on di/dt. Also, Gen-1 BiDFET hard turn-on switching losses have been reported to decrease with temperature, as forward voltage drop of JBS diode increases with temperature and reduces its junction capacitance [8]. Whereas, all commercial SiC MOSFETs switching losses are reported to increase with



(a)



(b)



(c)

Fig. 10: Switching energy variation with voltage and current at 25 °C: (a) Hard turn-on (E_{on}), (b) Hard turn-off (E_{off}), and (c) Total (E_{total}).

temperature in respective manufacturers provided datasheets. This is because P-i-N body diode stored charge increases with temperature, which causes increasing reverse-recovery losses during hard turn-on switching. Fig. 10 shows experimental results for hard turn-on (E_{on}), hard turn-off (E_{off}), and total (E_{tot}) switching energies for all FQS implementations at room temperature.

IV. Conclusion

This paper discusses the commutation schemes, switching transitions, and performance indices of a bidirectional commutation cell. The steady-state and switching performance of four-quadrant switches enabled by state-of-the-art commercially available SiC MOSFETs and the newly developed novel monolithic SiC-based Gen-1 and Gen-2 BiDFETs have been reported. SiC MOSFETs based bidirectional commutation cell PCB was found to have higher commutation inductance due to TO-247-4 package leads, the affect of which on switching waveforms and energy has been examined. The experimental results for switching transition times and body-diode turn-off behavior study will be provided in the future papers.

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