FET Junction Temperature Monitoring Using Novel On-Chip Solution

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***Abstract*—A novel junction temperature monitoring sensor is proposed and experimentally demonstrated for application in MOS-gate power devices. The sensor is created using the polycide gate electrode layer of the devices to create a temperature-sensitive resistor without any additional fabrication steps. The resistor is located on the field oxide with one end grounded at the device reference terminal to isolate it from the device current and voltage transients. It allows *in-situ* monitoring of the device junction temperature during active circuit operation. The technology has been implemented to monitor the junction temperature of Silicon Carbide Junction Barrier Schottky Field Effect Transistors (SiC JBSFETs) with the bi-directional FET (BiDFET).**

***Index Terms*—Bidirectional switches, SiC bidirectional FET, BiDFET, Junction Temperature, MOS Power devices, Silicon Carbide, Temperature sensing.**

I. Introduction

The junction temperature of power devices has been determined to be a dominant factor in determining their reliability during operation in power circuits. Manufacturers specify the maximum junction temperature in the device datasheets that should not be exceeded in applications. The device junction temperature is often estimated by computation of device power dissipation and thermal impedance. Engineers must include significant margins during design due to the in-exact method leading to reduction of the maximum power handled by the device. Sensing the device junction temperature can overcome this limitation.

This paper introduces a novel sensor that can be integrated into an MOS-gated power device to monitor its junction temperature. It is based on a resistor formed using the polycide gate electrode material used for MOS-gate power devices, such as Si MOSFETs, Si IGBTs, and SiC power MOSFETs. This sensor can be used for *in-situ* measurements of the junction temperature during active circuit operation without interference. This allows engineers to increase the power handled by the devices and optimize the control circuits to achieve superior performance without violating reliability limits.

The paper reviews previous approaches for measurement of junction temperature in power devices in section II. The limitations and complexity of implementation of each method is described. The new temperature sensing approach proposed in this paper is described in section III. Section IV provides a description of a temperature sensor design implemented on SiC BiDFET devices. Experimental data on temperature dependence of the sense resistor is provided with statistical distribution of its value across a wafer. The application of this technology for monitoring the *in-situ* junction temperature is demonstrated in section V using SiC BiDFETs.

II. Previous Temperature Sensing Approaches

The ability to monitor the junction temperature of power devices has been recognized for a long time. The reported approaches are reviewed in this section with a description of their limitations.

A. NTC Thermistor in Modules

A negative thermal coefficient (NTC) thermistor has been integrated into IGBT modules to monitor the temperature [1]. This approach allows monitoring the module baseplate temperature. The actual junction temperature for each of the multiple devices within the module can only be indirectly estimated.

B. Electromagnetic Radiation Method

The measurement of electromagnetic radiation (EMR) for a silicon IGBT has been proposed as an approach to estimate its junction temperature [2]. The EMR has been found to be function of the switching delay of the IGBT and proportional to the junction temperature. This approach requires a special laboratory set up with a loop antenna to gather the EMR signal. It does not directly sense the device junction temperature and cannot be used during actual power circuit operation in applications.

C. Infra-red radiation

The various temperature measurement approaches for power devices have been reviewed [3]. One method commonly used in a laboratory setting is measurement of infra-red radiation emanating from the power devices. A calibrated IR camera can assess the temperature at the surface of the package. The actual device junction temperature cannot be acquired unless the device die is exposed by removal of the packaging material. This is not suitable for the monitoring of devices when operating in power device applications.

D. Thermo-Sensitive Device Parameters

It is well known that the electrical characteristics of power devices vary with increasing temperature [4]. For example, the on-resistance of Si and SiC power MOSFETs increases with temperature by nearly 2-times from room temperature to 150 °C. The on-state voltage drop of Si IGBTs increases at their rated current but decreases at lower current levels [4]. The threshold voltage of all of these MOS-gated devices decreases with temperature. These device parameters can be used to assess the device junction temperature during operation in power devices.

There are many challenges for these approaches. For example, the room temperature values for on-state resistance of Si and SiC power MOSFETs can vary by up to 30 % according to their datasheets. A calibration of the on-state resistance at room temperature is therefore necessary for each device. In addition, the voltage at the drain terminal of the devices varies by a large value from the on-state voltage drop of about 1 V to the circuit supply voltage of typically 800 V. The on-state resistance sensed via the drain terminal must be isolated from the high voltages imposed at the drain.

The temperature dependence of the threshold voltage of Si IGBT has been used to estimate the junction temperature of devices within a module [5]. The method is sensitive to when the threshold voltage sensing is triggered. It works poorly when devices are connected in parallel. In addition, the threshold voltage varies between devices as supplied by the manufacturer.

Monitoring the turn-on and turn-off delay of devices has also been suggested as an approach to sense the temperature. This method is highly sensitive to the current level and DC bus voltage [3].

The challenges of the above approaches in the case of SiC power MOSFETs has been studied in detail and reported [6]. The rate of change of the on-resistance with temperature was reported to change with each new generation of the SiC power MOSFET product. It also depended on the drain current level used for sensing the resistance. Some bias-temperature-instability was also observed but may have been improved by manufactures since that paper was published.

E. P-Well Resistor

It is well established that the resistance of semiconductor layers increase with temperature due to a degradation of the bulk mobility [4]. A temperature dependent resistor can be integrated into the n-channel MOS-gated power device by creating a separate P-well. This has been experimentally evaluate for the SiC power MOSFET [7]. In the case of SiC, there is incomplete ionization of acceptors at room temperature making the resistance of p-type layers strongly dependent on temperature [8]. Implantation induced defects can also alter the conductivity of the layers. The positive bias used for sensing must be kept below 2 V to avoid injecting holes from the underlying junction into the n-drift region of the power MOSFET.

Most important issue with the P-well approach is that it is coupled to the power MOSFET drain via the junction capacitance. The static resistance of the sensor increases with drain bias by 16 % when the drain bias increases to 1000 V due to depletion of the P-well [8]. During switching of the drain voltage, a spike of 50 % is also observed for the sensor current due to the dV/dt. The accuracy of the temperature sensing was limited to 10 °C. The use of this approach for in-situ monitoring of the device junction temperature in a power circuit was not explored [7].

F. Polysilicon P-N Junction

Device junction temperature sensing has been demonstrated for the Si IGBT by using a P-N junction formed in a polysilicon layer [9]. In this work, a P-well that was connected to the emitter was formed under the sensor to isolate it from the collector voltage transients. The sensor was made of polysilicon in order to form a P-N junction. This involved additional processing steps to make a polysilicon layer because the gate electrode is fabricated using silicided polysilicon (polycide) to achieve a low internal gate resistance. Additional masking and ion-implant process steps are also required to introduce the P+ and N+ dopants into the polysilicon when making the P-N diode. Ten P-N diodes connected in series were utilized here. The on-state voltage across the diodes decreases with temperature allowing estimation of the junction temperature.

A similar approach was reported more recently for Si reverse conducting (RC) IGBTs in a module [10]. This approach was compared with the NTC thermistor installed in the module. The integrated sensor had an accuracy of +/- 6 °C due to variations in the properties of the polysilicon based p-n junction diodes. The integrated sensor was found to increase the maximum allowable current by 13 % when compared with the NTC thermistor. This establishes the importance of using an integrated sensor in the power devices.

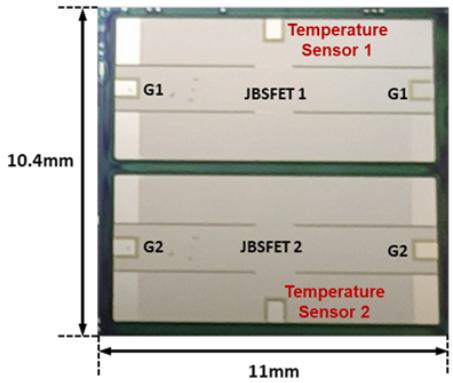
III. Novel Temperature Sensor Concept

From the discussion of the prior art in section II, it is clear that sensing and monitoring the junction temperature of power devices is a valuable asset for maximizing their performance in applications. Two previous methods that can perform this task are a semiconductor-based resistor and a polysilicon-based P-N junction diode. Both approaches require several additional masks and ion-implantation steps that add to the cost of implementation. The semiconductor-based resistance approach is also sensitive to the drain/collector bias which makes the sensing inaccurate.

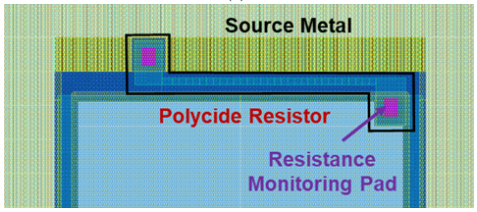
A new temperature sensing concept is described and experimentally demonstrated in this section. This method does not suffer from the short-comings of the previous approaches.

A. Polycide Temperature Sensor

The proposed temperature sensor is based on employing a polycide layer deposited on top of the field oxide [11]. The gate polycide layer that is utilized in MOS-gated power



(a)



(b)

Fig. 1. (a) Top view of BiDFET chip design with temperature sensing resistors integrated on both internal JBSFETs. (b) Temperature sensing resistor layout on chip.

devices, such as Si power MOSFETs, Si IGBTs, and SiC power MOSFETs for making products, can therefore be used without adding any process steps. The resistance of the polycide layer was discovered to increase with temperature in a reproducible manner allowing correlation of its resistance with the device junction temperature. One end of the polycide resistor is connected to the source/emitter electrode of the MOS-gated power device as a reference point for the resistor. This avoids the need for a separate bonding pad which would occupy space on the chip. The polycide temperature sensing resistor was implemented during the design of a 1.2 kV, 20 A SiC bi-directional FET (BiDFET). The BiDFET is comprised of two JBSFET working in tandem to achieve its bi-directional voltage blocking and current carrying capability [12], [13]. These devices are ideal for implementation of matrix converters [14].

The temperature sensing resistor was implemented as shown

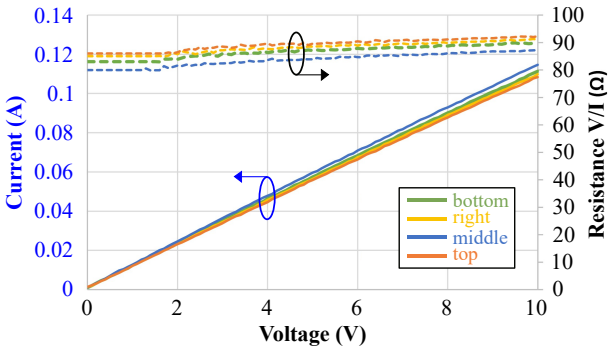
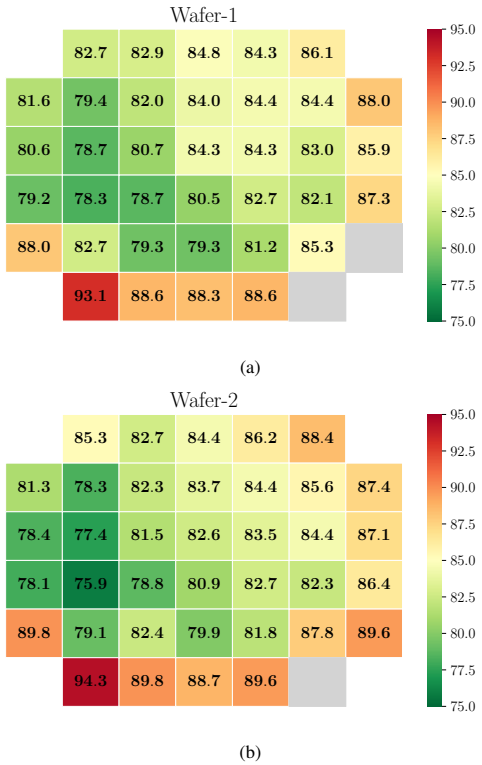


Fig. 2. Measured temperature dependence of sense resistor at four locations (bottom, right, middle, top) on a wafer.



(a)

(b)

Fig. 3. Measured temperature sense resistor values across two wafers: (a) Wafer-1 and (b) Wafer-2.

in Fig. 1a on both of the JBSFETs to monitor their temperature individually. The resistance of the sensor can be measured using a single wire bond to the pad because its other end is connected to the source terminal of the JBSFET.

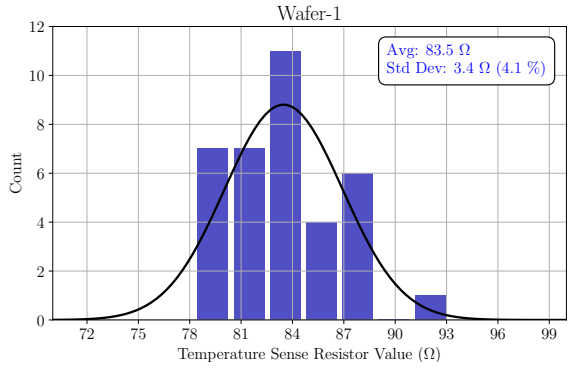
A closer look at the temperature sensing resistor is shown in Fig. 1b. The sheet resistance of the polycide was previously found to be about 3 Ω/sq. The polycide resistor was designed with 30 squares to obtain a resistance value of about 100 Ω.

B. Temperature Sense Resistor Characteristics

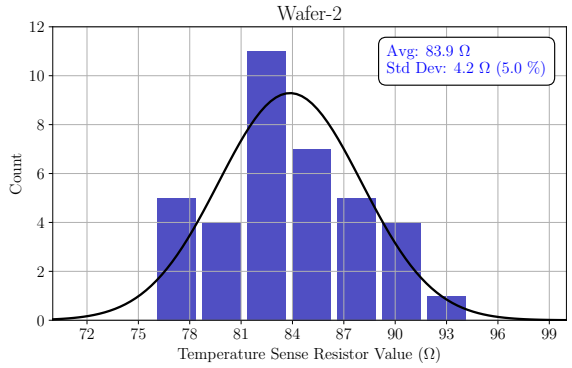
The BiDFET devices were manufactured in a 6-inch SiC foundry using the Gen-3 PRESiCE™ technology developed by NCSU [15]. The integrated temperature sensing resistors were created using the gate electrode material during the BiDFET fabrication without any additional masks or processing steps.

The measured i-v characteristics of the fabricated sense resistors at four locations (bottom, right, middle, top) on a wafer are shown in Fig. 2. The values vary from 87 to 92 Ω, a spread of 5.7 %. The value of the resistance is given as a function of current in the figure to show its linearity, i.e., no change in resistance with current level. This provides wide latitude during sense resistance monitoring in applications.

The distribution in the measured values for the temperature sense resistors is shown in Fig. 3 for two fabricated wafers as examples. The values vary from 78.3 to 93.1 Ω on wafer-1 and from 75.9 to 94.3 Ω on wafer-2. The highest values are outliers near the edge of the wafers. The statistical distribution of the measured temperature sense resistor values on both wafers is provided in Fig. 4. The average value for wafer-1 is 83.5 Ω and



(a)



(b)

Fig. 4. Measured statistical distribution of temperature sense resistor values across two wafers: (a) Wafer-1 and (b) Wafer-2. The blue bars depict the frequency of temperature sense resistor values within specified range of values, while the black line indicates a fitted normal distribution, scaled to the histogram's total count, representing the expected distribution if the data were perfectly normal.

for wafer-2 is 83.9 Ω a difference of only 0.5 %. The standard deviation for the data is only 5 % in spite of including the outliers. These measured results demonstrate that the proposed technology is manufacturable with good reproducibility across wafers and has a tight distribution within each wafer.

The variation of the sense resistor value was measured as a function of temperature using a hot-chuck on the probe station to adjust the wafer temperature. An example is shown in Fig. 5 for one of the sense resistors. The sense resistance value increased from 83.6 Ω at 25 °C to 96.1 Ω at 150 °C, a change of 15 %. This is a sufficiently large increase to allow extraction of the device junction temperature within 5 °C by measurement of the sense resistance value during circuit operation. The resistance increases linearly with temperature making the temperature extraction straightforward.

C. New Temperature Sensor Features

A novel temperature sensor has been described in previous sections based on utilizing the polycide gate electrode material used for MOS-gated power devices, such as Si MOSFETs, Si IGBTs, and SiC MOSFETs. Unique aspects of this approach are:

1) Sensor can be integrated within MOS-gated power devices with no additional masks or ion-implant steps, i.e., without adding any cost to the power devices;

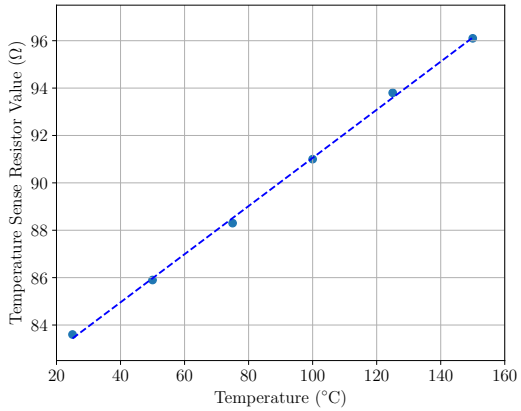


Fig. 5. Measured temperature dependence of sense resistor.

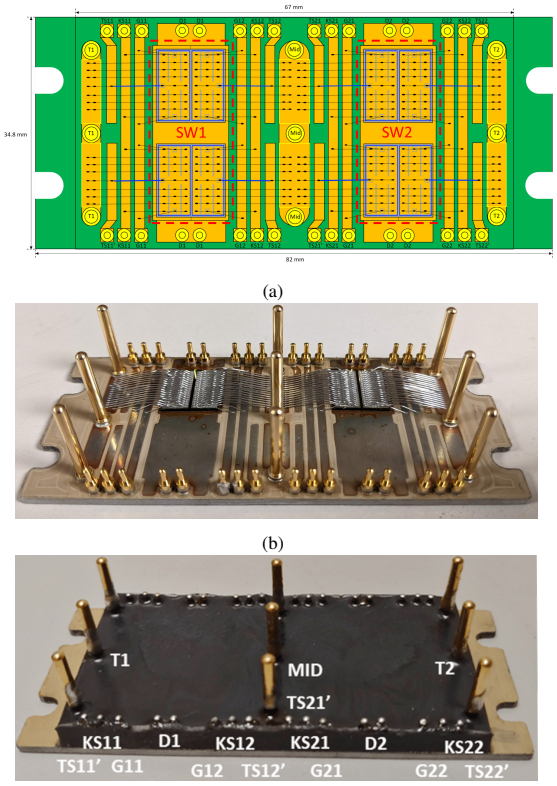
2) Sensor allows unique continuous or *in-situ* monitoring of power device junction temperature without interfering with its circuit operation;
3) Sensor can be located at any desired place on the SiC power MOSFET chip;
4) Multiple sensors can be integrated on the power devices to obtain the localized temperature.
5) Sensors can be located on each of the paralleled devices within modules to monitor the temperature of each of the devices.
6) Sensors on all the power devices can be monitored simultaneously while increasing the output power to obtain the maximum power capability when one of the devices arrives at the maximum allowable junction temperature;
7) Sensors on all the power devices with a power circuit can be monitored while changing the control strategy to avoid excessive temperature rise in one single device.

IV. Circuit Demonstration

A custom designed single-side cooled (SSC) half-bridge (HB) module having capability to house two BiDFETs in parallel per switch location was designed with an Epoxy-Resin Composite Dielectric (ERCD) substrate having an inherent Aluminum base plate [16]. The module's design includes three 15 mm cylindrical pins for each power terminal and shorter 5 mm pins for the gate, kelvin-source, common-drain, and temperature-sense terminals. While the power terminals are engineered for through-hole mounting, the signal pins are tailored for surface mounting. The module is equipped with a total of 8 temperature sense pins, allocating one for each JBSFET. The top views of the SSC HB BiDFET module packaging design, before encapsulation, and post encapsulation, are shown in Fig. 6. For this paper, a half-bridge module having single BiDFET die per switch location is utilized.

A. Temperature Sensor Circuitry

The designed temperature sensor circuitry includes a current-source, I_{ref}, which feeds the JBSFET temperature sense resistor, R_{temp}. This setup, depicted in Fig. 7a, generates a voltage, V_{temp}. To amplify only the variations in V_{temp}, the circuit employs an op-amp (OPA350UAG4) based design

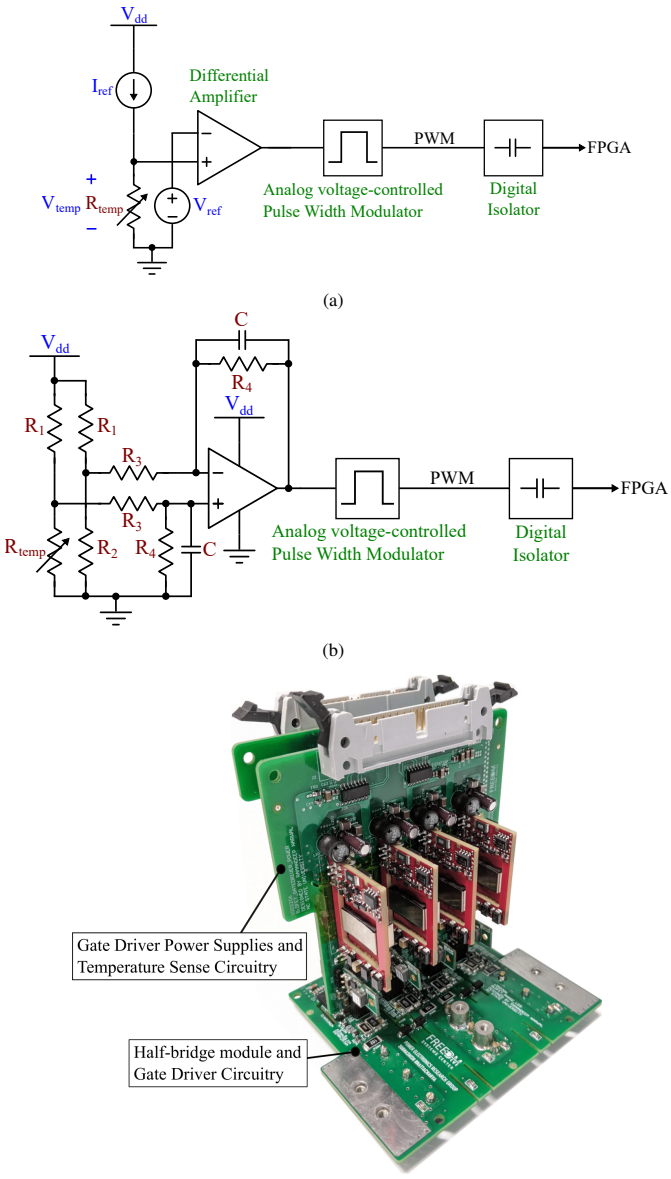


(a)

(b)

(c)

Fig. 6. BiDFET half-bridge module (a) package design, (b) before encapsulation, and (c) after encapsulation.



(a)

(b)

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Fig. 7. (a) Equivalent diagram of temperature sense circuitry, (b) Practical implementation of temperature sense circuitry, and (c) Hardware implementation of gate driver power supplies and temperature sense circuitry for BiDFET based half-bridge module.

to amplify the differential between V_{temp} and a reference voltage, V_{ref}, resulting in an output voltage range of 0 to 1 V at the op-amp's output. This voltage is then converted into a variable duty cycle Pulse Width Modulated (PWM) signal by an analog voltage-controlled pulse width modulator (LTC6992IS6-2TRMPBF). The PWM signal is transmitted from the high-voltage side to the FPGA on the control signal side through a Digital Isolator (ISO7820DWW). Within the FPGA, the duty cycle of the PWM signal is computed and then correlated to a temperature value, based on a predefined temperature-duty cycle relationship.

In the practical implementation, the current source (I_{ref}) and the reference voltage (V_{ref}) are established using resistor circuits, as depicted in Fig. 7b. However, for enhanced precision, current mirror circuits and reference voltage generators may be employed. With the current setup, the precision achieved was found to be satisfactory for measuring temperatures within a 5 °C range. The voltage, V_{dd} (= 5 V), is derived from the gate driver's positive power supply voltage (≈ 20 V). To optimize space and reduce noise, the entire temperature sense circuitry can be integrated into an Application-Specific Integrated Circuit (ASIC). A hardware prototype of the power PCB, which includes a BiDFET half-bridge module and gate driver circuitry, along with a daughterboard containing gate power supplies (12 V to +20/ -5 V) and temperature sensing circuits for all 8 JBSFETs, is illustrated in Fig. 7c.

B. Temperature Sensor Calibration with Hot Plate

To calibrate the temperature sensors in the BiDFET module, the module was uniformly heated using a hot-plate. The procedure ensured that each BiDFET reached a thermal steady-state. This condition implies that the temperatures of the module's baseplate and the JBSFETs junctions were equalized. The hot plate temperature was varied from ambient room temperature to 140 °C. During this process, both the values of the temperature sense resistors and the output duty cycles of the sensors were recorded. The data for two JBSFETs in the tested BiDFET module, as shown in Fig. 8b and Fig. 8c, substantiates the linear correlation between the temperature, the resistance values of the temperature sense resistors, and the sensor outputs. This correlation confirms the feasibility

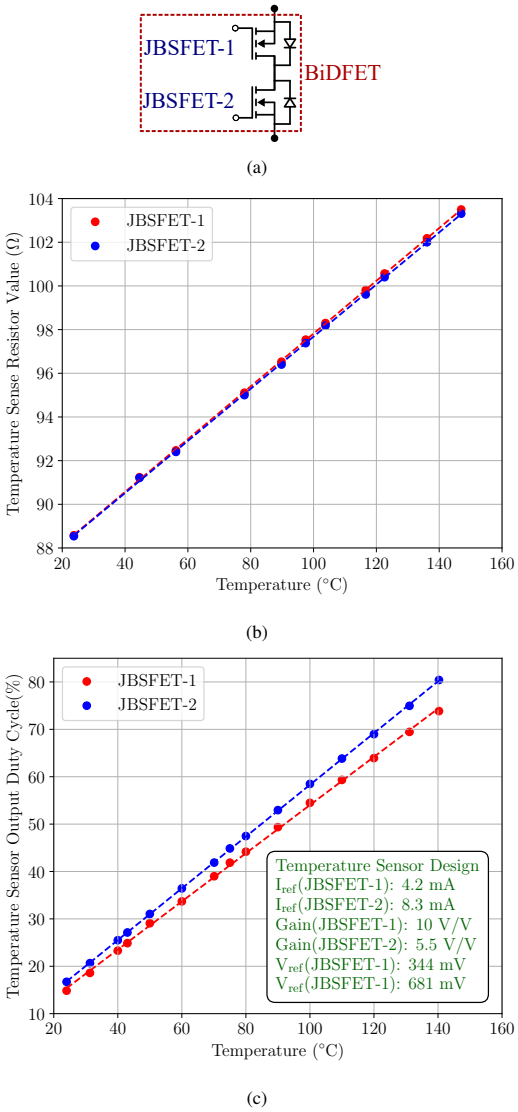

Fig. 8. (a) BiDFET equivalent diagram having two JBSFETs connected back-to-back in common-drain configuration. (b) Measured temperature dependence of temperature sense resistors of both JBSFETs in the BiDFET under test. (c) Measured temperature dependence of temperature sensors output duty cycle.

of translating the sensor output duty cycle readings into temperature values in power converters.

The temperature sensors are designed to have a 50 kHz sampling rate. The sensors output at 24 °C and 122 °C are shown in Fig. 9. For a temperature variation from 24 °C to 140.3 °C, the duty cycle of the JBSFET-1 temperature sensor varies from 14.8 % to 72.4 %, and that of the JBSFET-2 temperature sensor varies from 16.7 % to 79.4 % The calculated sensitivities are approximately 0.495 %/°C for JBSFET-1 and 0.539 %/°C for JBSFET-2, indicating the degree of change in duty cycle per unit change in temperature.

Furthermore, the temperature sensor circuits for the two JBSFETs were engineered with different current source, I_{ref} values: 2.8 mA and 5.5 mA, respectively. To ensure the op-amp output voltage remained within the range of 0 to 1 V, the op-amp gains were accordingly adjusted to 10 V/V and 5.5 V/V. This design strategy highlights the flexibility of

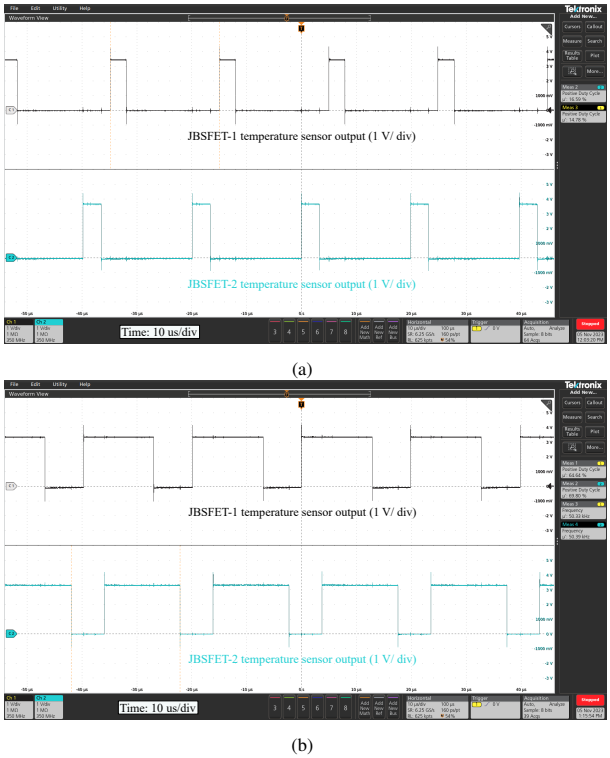

Fig. 9. Measured temperature sensors outputs for JBSFET-1 and JBSFET-2 at junction temperature of (a) 24 °C and (b) 122 °C.

the temperature sensor circuits, which can be customized to suit specific operational parameters, including mitigating noise levels influenced by the layout of the PCB.

C. Testing with pulsed current source

The dynamic response of the temperature sensor was evaluated by applying a current source power supply across the BiDFET terminals as illustrated in Fig. 10a. In this test, JBSFET-1 was kept in an OFF state, which allowed its anti-parallel Junction Barrier Schottky (JBS) diode to conduct the current. In contrast, JBSFET-2 was maintained in an ON state, enabling current conduction through its channel. Due to the higher voltage drop across the JBS diode, JBSFET-1 is expected to experience greater power loss and, consequently, a higher temperature compared to JBSFET-2. The junction temperatures of JBSFETs were monitored using the calibrated temperature sensors and their outputs were recorded with an oscilloscope (Tektronix MSO58). The baseplate temperature of the BiDFET module was simultaneously measured using a FLK-T3000 wireless temperature module. The thermocouple was placed on the baseplate at a position directly beneath the BiDFET location. The per-second baseplate temperature data was recorded using the Fluke Connect™ app.

The temperatures of JBSFET-1, JBSFET-2, and the baseplate of the BiDFET module were measured over a 200-second duration under a 15 A current source pulse, as illustrated in Fig. 10b. Consistent with our hypothesis, JBSFET-1 exhibited a higher temperature than JBSFET-2. Additionally, the baseplate temperature of the module was not only lower but also demonstrated a slower response, which can be attributed to the

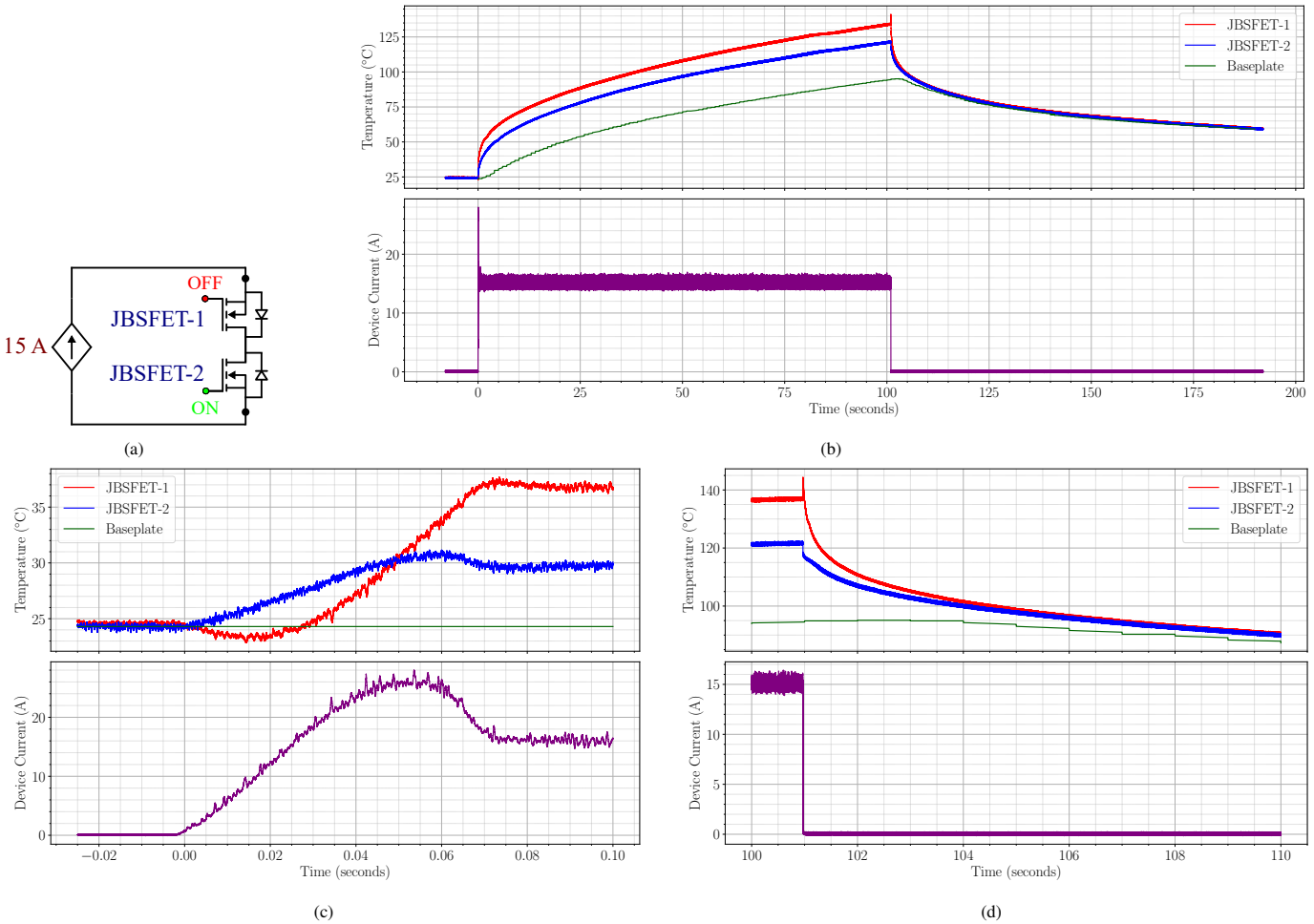

Fig. 10. (a) Test setup for evaluating the BiDFET temperature sensors using a controlled 15 A current source. Measured temperatures of JBSFETs junctions and module baseplate over different time intervals: (b) 200 seconds for an overall view, (c) a 100 milliseconds zoom-in at the rising edge of the current source, highlighting the dynamic response, and (d) a 10 seconds zoom-in at the falling edge of the current source to observe the cooling behavior.

inherent thermal capacitances of the system. Fig. 10c shows the rising edge of device current which peaks to around 26 A, before settling to 15 A. The impact of this transient current peak is markedly evident in the temperature profiles of the JBSFETs junctions. In contrast, the temperature of the BiDFET module's baseplate exhibits a delayed response. These observations underscore the significant advantages offered by the integration of on-chip temperature sense resistors. Notably, these resistors facilitate not only the precise measurement of the FET junction temperatures but also ensure a markedly faster response time. This rapid response is particularly crucial in scenarios involving surge current, inrush current, and transient thermal runaway conditions.

After the 15 A current source was turned off, the junction temperatures of the JBSFETs and the baseplate temperature of the BiDFET module began to converge as the system approached a new steady state. During this phase, the temperatures of the JBSFETs quickly equalized, and then the temperatures of both the JBSFETs and the baseplate closely aligned and gradually declined towards the steady-state temperature.

The analysis of the JBSFET temperature profiles reveals a notable responsiveness to even microsecond-range fluctuations in the current profile. However, a discernible delay is observed in this response, which could potentially be attributed to the combined latency effects of various components in the circuit, such as the op-amp filter, the pulse-width modulator, the digital isolator, and the low-pass filter employed for duty cycle measurement with the oscilloscope.

An interesting dynamic is observed in the case of JBSFET-1 during rapid increases in device current: the junction temperature initially decreases before showing an increase. Conversely, for a sharp decrease in device current, the JBSFET-1 junction temperature exhibits an initial increase before decreasing. This phenomenon is likely a consequence of parasitic inductances within the measurement circuitry and needs to be investigated further. Such a pattern is not evident in JBSFET-2 temperature sensor output, suggesting the influence of temperature sensor circuitry design choices on these observations.

V. Conclusion

This paper introduces a novel junction temperature monitoring sensor for MOS-gate power devices, utilizing the polycide

gate electrode layer to create temperature-sensitive resistor without additional fabrication steps. This sensor enables *in-situ* monitoring of junction temperatures in devices such as Si/SiC MOSFETs, JBSFETs and BiDFETs, enhancing their operational reliability. Its integration into existing device architectures without incurring extra manufacturing costs, its capability for continuous temperature monitoring without impacting circuit operation, and the flexibility in sensor placement on SiC power MOSFET chips are its standout features. This technology also allows the integration of multiple sensors for localized temperature measurements and simultaneous monitoring of paralleled devices within modules, which is crucial for optimal power management and preventing overheating in individual devices.

The polycide temperature sensing resistor was incorporated during the design of a 1.2 kV, 20 A SiC bi-directional FET (BiDFET). The statistical analysis of the measured temperature sense resistor values across two wafers indicates excellent reproducibility and a tight distribution within each wafer.

Furthermore, a temperature sensor circuitry design is provided for sensing the change in resistance of the temperature sense resistor. The sensors undergo initial calibration utilizing a hotplate, followed by a dynamic performance test. This test measures the junction temperatures of two JBSFETs in a BiDFET, comparing them with the baseplate temperature under a 15 A current pulse over 200 seconds. The demonstrated effectiveness of this sensor in precise and real-time monitoring of the device junction temperature marks a significant advancement in power electronics, offering a practical and adaptable solution for enhancing the performance and safety of MOS-gate power devices during continuous operation in power converters.

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